IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An electronic apparatus having a semiconductor integrated circuit having a first circuit and a second circuit, ~~each of the first circuit and~~ the second circuit having a normal operation state and a standby state, the electronic apparatus comprising:

power controlling means for supplying power to the first circuit and the second circuit in the normal operation state and for supplying power to only the first circuit in the standby state;

first and second clock generators disposed in the first circuit and configured to generate first and second clock signals;

a third clock generator disposed in the second circuit and configured to generate a third clock signal;

clock controlling means for controlling a generation of ~~a~~ first, ~~clock and a~~ second and third clock signals so as to generate the first clock signal, ~~and~~ the second clock signal, and the third clock signal in the normal operation state and only the first clock signal in the standby state;

a first register that is disposed in the first circuit and operated with the first clock signal;

a second register that is disposed in the first circuit and operated with the second clock signal; and

controlling means for copying contents that are set to the first register to the second register when the state of the second circuit changes from the standby state to the normal operation state, wherein

the second clock signal is provided to the first circuit and the second circuit, and the third clock generator generates the third clock signal only when the third clock generator receives the second clock signal.

Claim 2 (Currently Amended): The electronic apparatus as set forth in claim 1, wherein the frequency of the first clock signal is lower than the frequency of the second clock signal.

Claim 3 (Original): The electronic apparatus as set forth in claim 1, wherein data is set to the second register not through the first region in the normal operation state.

Claim 4 (Original): The electronic apparatus as set forth in claim 1, wherein the contents of the second register are read by a CPU disposed in the second circuit.

Claim 5 (Original): The electronic apparatus as set forth in claim 1, wherein information of an event is set from an input device disposed outside the semiconductor integrated circuit to the first register.

Claim 6 (Original): The electronic apparatus as set forth in claim 1, wherein the power is supplied from a battery.

Claim 7 (Currently Amended): The electronic apparatus as set forth in claim 1, wherein the contents that have been set to the first register are copied to the second register in parallel in one period of the first clock signal.

Claim 8 (Currently Amended): A method for controlling a semiconductor integrated circuit having a first circuit and a second circuit, ~~each of the first circuit and~~ the second circuit has a normal operation state and a standby state, the method comprising the steps of:

controlling power supplied to the first circuit and the second circuit so as to supply the power to the first circuit and the second circuit in the normal operation state and the power to only the first circuit in the standby state;

controlling generation of a first clock signal,~~and~~ a second clock signal, and a third clock signal so as to generate the first clock signal, ~~and~~ the second clock signal, and the third clock signal in the normal operation state and to generate only the first clock signal in the standby state;

generating the third clock signal only when a second clock signal generated by the first circuit is received by the second circuit;

providing the second clock signal to the first circuit and the second circuit; and

copying contents that are set in ~~the~~ a first register that is disposed in the first circuit and operated with the first clock signal to a second register that is disposed in the first circuit and operated with the second clock signal when the state of the second circuit changes from the standby state to the normal operation state.